Remarks

Applicant respectfully traverses all of the Section 102(e) and 103(a) rejections because Ayadi (U.S. 6,782,331) fails to teach deciding based on the generated quality test-data whether other semiconductor devices on the wafer are to be tested or not as in the claimed invention. For the reasons and arguments set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The non-final Office Action dated August 21, 2006 indicated the following: claims 1-7 stand rejected under 35 U.S.C. § 112(2) as being indefinite; claims 1-7 also stand rejected under 35 U.S.C. § 112(2) as being incomplete; claims 1-5 and 7-10 stand rejected under 35 U.S.C. § 102(e) over Ayadi; and claim 6 stands rejected under 35 U.S.C. § 103(a) over Ayadi in view of Brady *et al.* (U.S. 6,236,223).

Applicant traverses the Section 112(2) rejections of claims 1-7 on page 2, paragraph 2 of the Office Action, because the claims do particularly point out and distinctly claim the subject matter that Applicant regards as the invention. The Office Action fails to provide any detail concerning the reasons for the rejections or anything in support of the rejections. As such, Applicant is unable to determine the propriety of the rejections. Accordingly, the rejections are improper and Applicant requests that they be withdrawn. Should the Section 112(2) rejections of claims 1-7 be maintained, Applicant requests an explanation elaborating the reason for the rejections and an opportunity to respond thereto.

Applicant traverses the Section 112(2) rejections of claims 1-7 because "step 22" is merely one embodiment of the claimed invention. In step 22, the result of the sampling measurement 20 is considered and analyzed (*see, e.g.*, paragraph 0076). As indicated in Applicant's Specification, Fig. 2 which depicts step 22 is but one example embodiment of the present invention. "In determining whether an unclaimed feature is critical, the entire disclosure must be considered. Features which are merely preferred are not to be considered critical. *In re Goffe*, 542 F.2d 564, 567, 191 USPQ 429, 431 (CCPA 1976). Broad language in the disclosure, including the abstract, omitting an allegedly critical feature, tends to rebut the argument of criticality." M.P.E.P. § 2164.08(c). Applicant's Abstract does not recite the alleged essential step 22. Moreover, one of skill in the art would understand that in claims 1 and 5 the test-data is generated and a decision is made based on that test-data. Therefore, the Section 112(2) rejections of claims 1 and 5, as

well as the rejections of claims 2-4 and 6-7 that depend from claims 1 and 5, are improper and Applicant requests that they be withdrawn

Applicant traverses the Section 102(e) rejections of claims 1-5 and 7-10 because the cited portions of the Ayadi reference fail to correspond to all of the claimed limitations. Regarding claims 1 and 5, the Office Action fails to cite any reference that corresponds to claimed limitations directed to deciding based on the generated quality test-data whether other semiconductor devices on the wafer are to be tested or not tested. The Ayadi reference is directed towards a graphical user interface that allows a user to select which ICs 44 on a semiconductor wafer are to be tested (*see, e.g.*, Abstract; Figs. 2 and 8; col. 4, lines 46-61). The cited portions of the Ayadi reference (*i.e.*, col. 5, lines 25-34) teach selecting ICs for testing and keeping track of whether all selected ICs have been tested, not deciding which ICs to test based on the results of previously tested ICs. Accordingly, the Office Action fails to show that the Ayadi reference teaches or suggests correspondence to the claimed step of deciding whether devices on the wafer are to be tested or not based on the results of the testing.

Regarding claim 8, the Office Action fails to cite any reference that corresponds to claimed limitations directed to deciding means for deciding, based on the quality test results, whether other semiconductor deceives on the wafer are to be tested or not tested. As discuss above, the Office Action has failed to show how the Ayadi reference teaches or suggests correspondence to the step of deciding whether or not to test devices on the wafer based on the test results. Therefore, the Office Action has failed to show how the Ayadi reference teaches or suggests a deciding means as claimed in claim 8.

Without a presentation of correspondence to each of the claimed limitations, the Section 102(e) rejections cannot be maintained. Accordingly, the rejections of independent claims 1, 5 and 8, as well as the rejections of claims 2-4, 7 and 9-10 that depend from claims 1, 5 and 8, are improper and Applicant requests that they be withdrawn. Notwithstanding the impropriety of the rejections of all of the dependent claims as related to the independent claims above, the limitations of certain dependent claims are addressed further below.

Regarding claim 4, cited portions of the Ayadi reference fail to correspond to claimed limitations directed to the limited number of devices being located on the wafer

as determined by a circular pattern, an X-cross pattern, a pattern in the form of a plus-sign or a spiral pattern. The cited portion of the Ayadi reference (*i.e.*, Fig. 8) shows that all of the ICs 44 are selected for testing which is indicted by a check mark (*see, e.g.*, col. 4, lines 51-57). The cited portions of the Ayadi reference fail to teach any of the claimed patterns. Therefore, the Section 102(e) rejection of claim 4 is improper and Applicant requests that they be withdrawn.

Applicant traverses the Section 103(a) rejection of claim 6 because the Ayadi reference does not correspond to all of the claimed limitations. The cited portions of the Brady reference do not teach that the shifting of the spatial pattern comprises a rotation of the pattern between wafers as required by the claimed limitations. The Brady reference teaches that a carriage assembly 412 can be rotated thereby allowing each of the ICs 418 on a wafer to be tested (*see, e.g.*, Fig. 4A; col. 6, lines 54-65). Applicant fails to see how rotating a wafer to be able to test each of the ICs 418 as taught by Brady in any way teaches rotating the pattern of the limited number of devices to be tested between wafers, thereby testing substantially all of the devices located on a wafer over the testing of a plurality of wafers. Accordingly, the Section 103(a) rejection of claim 6 is improper and Applicant requests that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the patent agent overseeing the application file, Peter Zawilski, at (408) 474-9063.

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